REMARKS

The Examiner is thanked for the indication that claims 11-14 would be allowable if rewritten to overcome informalities. The Examiner also is thanked for the indication that claims 15-18 would be allowable if rewritten or amended to overcome the rejections under 35 U.S.C. §112, second paragraph.

Claims 11-18 are presented for reconsideration. Claims 11 and 15 are independent. Claims 12-14 and 16-18 are dependent. Claims 11 and 15 have been amended. These changes are believed to introduce no new matter, and their entry is respectfully requested. Based on the above Amendment and the following Remarks, the Applicants respectfully request that the Examiner reconsider and withdraw all rejections and pass claims 11-18 to allowance.

Rejection to Claim 15 Under 35 U.S.C. §112, First Paragraph

In paragraph 2, the Examiner rejected claim 15 under 35 U.S.C. §112, first paragraph as failing to provide proper "antecedent basis" for the claimed subject matter. The rejection as applied to specific language is addressed in turn below.

The Examiner asserts that there is no support in Applicants Disclosure for "a first gate structure formed atop said n-well" as recited in claim 15, line 7. Applicant respectfully traverses the rejection. Applicant respectfully directs the Examiner's attention to page 3, lines 22-25 and to Figure 1, which describe in detail at least one embodiment of "a first gate structure formed atop said n-well." As Applicants have specifically pointed out support in the Disclosure for the language recited, Applicant respectfully requests that the Examiner reconsider and remove the rejection.

The Examiner asserts that there is no support in Applicants Disclosure for "a second gate structure formed atop said n-well" as recited in claim 15, line 10. Applicant respectfully traverses the rejection. Applicant respectfully directs the Examiner's attention to page 7, lines 9-33, page 8, lines 20-21, Figure 10, and Figure 10A, which

describe in detail at least one embodiment of "a second gate structure formed atop said n-well." As Applicants have specifically pointed out support in the Disclosure for the language recited, Applicant respectfully requests that the Examiner reconsider and remove the rejection.

The Examiner asserts that there is no support in Applicants Disclosure for "a n+ structure being the output of said NAND logic circuit" as recited in claim 15, line 14. Applicant respectfully traverses the rejection. Applicant respectfully directs the Examiner's attention to page 7, lines 13-26, which describes in detail at least one embodiment of "a n+ structure being the output of said NAND logic circuit." As Applicants have specifically pointed out support in the Disclosure for the language recited, Applicant respectfully requests that the Examiner reconsider and remove the rejection.

The Examiner asserts that there is no support in Applicants Disclosure for "said second switch also electrically connected to said n+ structure" as recited in claim 15, lines 22-23. Applicant has amended claim 15 to delete the language "said second switch also electrically connected to said n+ structure," which deletion renders the rejection moot. Accordingly, Applicant respectfully requests that the Examiner reconsider and remove the rejection.

Objection to Claims 11 and 15

In paragraph 4, the Examiner objected to claims 11 and 15 asserting that the phrase "said first gate structure being the second input" is misdescriptive. Applicant has amended claims 11 and 15 to accommodate the Examiner's objection. Accordingly, Applicant respectfully requests that the Examiner reconsider and remove the objection.

Rejection to Claim 15 Under 35 U.S.C. §112, Second Paragraph

In paragraph 6, the Examiner rejected claim 15 under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim what

the Applicant regards as the invention. The rejection as applied to specific language is addressed in turn below.

The Examiner asserts that the phrase "a first gate structure formed atop said n-well" as recited in claim 15, line 7 is misdescriptive because it is inconsistent with Figure 10A, which does not show "a first gate structure formed atop said n-well." Applicant respectfully traverses the rejection and requests that the Examiner again look at Figure 10A, which shows "a first gate structure formed atop said n-well." Applicant has specifically pointed out support in Figure 10A for the language recited, Applicant respectfully requests that the Examiner reconsider and remove the rejection.

The Examiner asserts that the phrase "a second gate structure formed atop said n-well" as recited in claim 15, line 10 is misdescriptive because it is inconsistent with Figure 10A, which does not show "a second gate structure formed atop said n-well" Applicant respectfully traverses the rejection and requests that the Examiner again look at Figure 10A, which shows "a second gate structure formed atop said n-well." Applicant has specifically pointed out support in Figure 10A for the language recited, Applicant respectfully requests that the Examiner reconsider and remove the rejection.

The Examiner asserts that the phrase "a n+ structure being the output of said NAND logic circuit" as recited in claim 15, line 14 is misdescriptive because "a p+ structure is the output of said NAND logic circuit." Applicant has amended claim 15 to delete the language "said n+ structure being the output of said NAND logic circuit" and added the language "said p+ structure being the output of said NAND logic circuit," which amendment accommodates the rejection. Accordingly, Applicant respectfully requests that the Examiner reconsider and remove the rejection.

The Examiner asserts that the phrase "said second switch also electrically connected to said n+ structure" as recited in claim 15, line 14 is misdescriptive because Figure 10A does not show and the written description does not disclose "said second switch also electrically connected to said n+ structure." Applicant has amended claim 15

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to delete the language "said second switch also electrically connected to said n+ structure," which amendment accommodates the rejection. Accordingly, Applicant respectfully requests that the Examiner reconsider and remove the rejection.

CONCLUSION

Applicant submits that all grounds for objection and rejection have been properly traversed, accommodated, or rendered moot. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections and pass claims 11-18to allowance. The Examiner is invited to telephone the undersigned representative if the Examiner believes that an interview might be useful for any reason.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

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on December 6, 2002
Date of Deposit

Luci Arevalo
Name of Person Mailing Correspondence

Signature Date

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VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

11. (Amended) A NAND logic circuit having a first input and a second input, comprising:

a semiconductor substrate;

an insulator formed on said semiconductor substrate;

a semiconductor layer formed on said insulator layer;

a p-well formed in said semiconductor layer;

a first gate structure formed atop said p-well, said first gate structure being the first input and being formed from a thin gate oxide layer underneath a conductive layer;

a second gate structure formed atop said p-well, said [first] second gate structure being the first input and being formed from a thin gate oxide layer underneath a conductive layer;

a p+ structure formed adjacent to a first edge of said first gate structure and said second gate structure, said p+ structure being the output of said NAND logic circuit;

an n+ structure formed adjacent to a second edge of said first gate structure and said second gate structure;

a first switch formed in said semiconductor layer, said first switch electrically connected to said first input; and

a second switch formed in said semiconductor layer in series to said first switch and electrically connected to said second input, said second switch also electrically connected to said p+ structure.

15. (Amended) A NAND logic circuit having a first input and a second input, comprising:

a semiconductor substrate;

an insulator formed on said semiconductor substrate;

a semiconductor layer formed on said insulator layer;

a n-well formed in said semiconductor layer;

a first gate structure formed atop said n-well, said first gate structure being the first input and being formed from a thin gate oxide layer underneath a conductive layer;

a second gate structure formed atop said n-well, said [first] second gate structure being the first input and being formed from a thin gate oxide layer underneath a conductive layer;

a n+ structure formed adjacent to a first edge of said first gate structure and said second gate structure[, said n+ structure being the output of said NAND logic circuit];

a p+ structure formed adjacent to a second edge of first gate structure and said second gate structure, said p+ structure being the output of said NAND logic circuit;

a first switch formed in said semiconductor layer, said first switch electrically connected to said first input; and

a second switch formed in said semiconductor layer in series to said first switch and electrically connected to said second input[, said second switch also electrically connected to said n+ structure].

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